Notice of Allowability	Application No.	Applicant(s)	
	10/796,475	TRIMBERGER ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/19/06*.

2. ☒ The allowed claim(s) is/are *1,3-17 and 19-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTQ-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

DETAILED ACTION

Applicant's response was received and entered April 24, 2006.

- Claims 1, 3-17 & 19-31 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach the following limitations:

The present invention includes an error correction system and method for a programmable logic device having a frame circuit arranged to retrieve data from each column of configuration memory of the PLD, a check memory for storage of a plurality of check words, a buffer circuit coupled to the check memory and to the frame circuit, the buffer circuit arranged to assemble blocks of data from data retrieved by the frame circuit, and from corresponding check words in the check memory, a mask memory specifying variant memory cells of the configuration memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD, and a mask circuit coupled to the mask memory and to the buffer circuit and arranged to substitute in the blocks of data a constant value for the value of each variant memory cell, a plurality of storage elements, and a check circuit coupled to the plurality of storage elements and to the buffer circuit, the check circuit arranged to check each block with an error correcting code and store data indicating detected errors in the plurality of storage elements.

The prior arts of record Quayle et al. US Pat no. 6,694,464, Nishihara US Pat no. 6,304,101 and Raza US Pat no. 5,943,488 teach a programmable logic

circuit having a circuit element and a configuration memory connected to the circuit element in which a programmable logic device is configured based upon circuit information written to the configuration memory, a circuit information storage different from the configuration memory that stores plural circuit information pieces for sequentially configuring plural circuits in the programmable logic circuit, a circuit information writer that writes plural circuit information pieces to the circuit information storage, a circuit information editor that generates the circuit information of one circuit specified to be generated in the programmable logic circuit and specified in specification information using one or plural circuit information pieces out of plural circuit information pieces stored in the circuit information storage, and a controller that writes the circuit information of the circuit generated by the circuit information editor to the configuration memory (Nishihara). Further Raza, teaches a mask programmed device implementing a logic function, comprising the steps of creating a field-programmable device or array and a mask-programmable device or array, determining an interconnect map that would implement the logic function on the field programmable device or array, and implementing the interconnect map on the mask programmable device or array by mask programming the interconnects determined in the interconnect map onto the mask programmable device or array. Hence, both inventions teach programming a programmable logic device, but they do not specifically teach a masked memory specifying the exact locations of the variant memory cells within a programmable logic device, initially allowing the values of those programmable cells to vary, and then selectively writing constant data within chosen variant

cells. The prior art of record merely writes data on the programmable logic device as a whole, in order to make the programmable logic device to implements a function as a whole.

Hence, the prior arts of record fail to anticipate or render obvious the claimed inventions. Thus claims 1, 3-17 & 19-31 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197

(toll-free).

S.S

Saqib Siddiqui
Art Unit 2138
09/13/2006

GUY LAMARRE
PRIMARY EXAMINER